DIOPHANTINE
FREQUENCY SYNTHESIS

The Invasion of Number Theory
to
Frequency Synthesis Systems

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April 20th 2006

Presented at the APPLIED MATHEMATICS AND STATISTICS department, J.H.U.

The talk presents part the of material published at:

1. P. Sotiriadis, *"Diophantine Frequency Synthesis"*, IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control (To appear).

2. P. Sotiriadis, *"Diophantine Frequency Synthesis; A Number Theory Approach to Fine Frequency Synthesis"*, IEEE International Frequency Control Symposium 2006, (June 5th 2006).

3. *"Prime-Rational Frequency Synthesis Method and Frequency Synthesizers"*, P. Sotiriadis, M.L. Edwards, G. Weaver, S. Cheng, D. Loizos, M. Wesley, C. Haskins, [Patent Pending – with APL].

Refs. [1] *and* [2] *are available upon request: pps@jhu.edu*

3W

Who: Paul P. Sotiriadis
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What: High Frequency Circuits: Design, Modeling, Optimization
- Analog, RF, microwave, interconnects, computational
- Integrated, some discrete prototypes

Where: Lab is at Stieff bldg (off campus ~ 1mile, take shuttle)
Stieff 150-151
Lab's # 410-516-3801
Administrative assistant: Mrs. Catonya Lester : 410-516-4276

Acknowledgements –part 1

- Profs. Daniel Naiman & James Fill

  for inviting me to give this talk

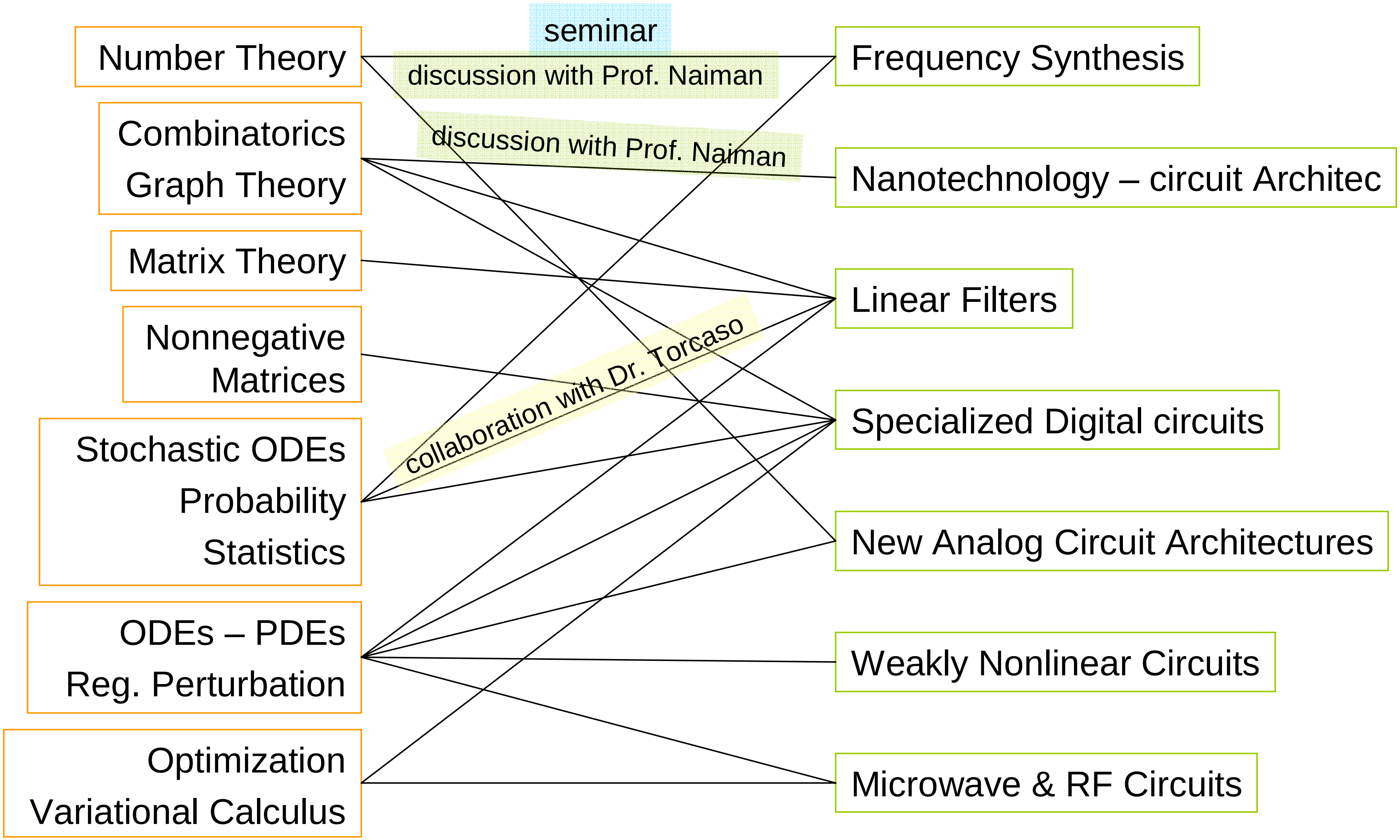
- Prof. Daniel Naiman

  for the long technical discussions

- Dr. Fred Toscaso

  for our ongoing collaboration

Applied Math Involved in my Research



please EMAIL me…

- If you are interested in using Applied Math to solve some real-world circuits' problems

- Or, if you find any error(!) in the "Diophantine Frequency Synthesis" paper available to you after the talk.

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- * *P. Sotiriadis, "Diophantine Frequency Synthesis", IEEE Transactions on UFFC, (To appear).*
- *"Prime-Rational Frequency Synthesis Method and Frequency Synthesizers", P. Sotiriadis, M.L. Edwards, G. Weaver, S. Cheng, D. Loizos, M. Wesley, C. Haskins, patent pending*

DIOPHANTINE
FREQUENCY SYNTHESIS

Acknowledgements –part 2

- The APL – JHU “Disciplined Ultra Stable Oscillator” TEAM

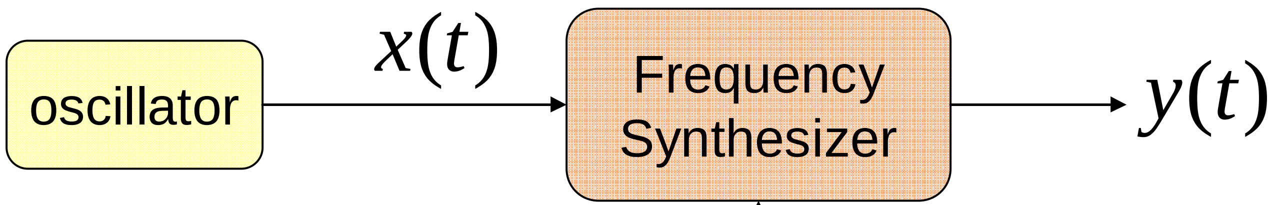
APL: *Dr. Lee Edwards*
Greg Weaver
Sheng Cheng
Wes Millard
Chris Haskins

JHU: *Dimitri Loizos*
Dr. Paul Sotiriadis

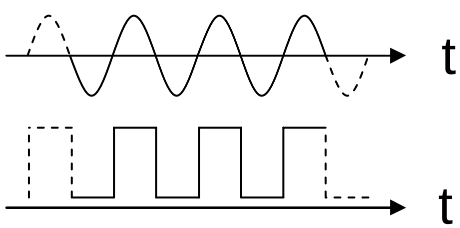
Outline of the Talk

- Frequency Synthesis & Fine Frequency Synthesis?
- Why / where?
- what / why DFS?
- DFS – how things started
- Frequency Synthesis 101
- Diophanthine Frequency Synthesis
- Open questions

What is Frequency Synthesis?



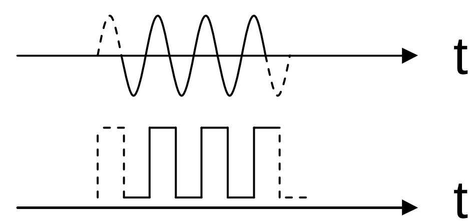
It generates
a periodic signal of
FIXED frequency f_{osc}



E.g. $x(t) = \cos(2\pi f_{osc} t)$

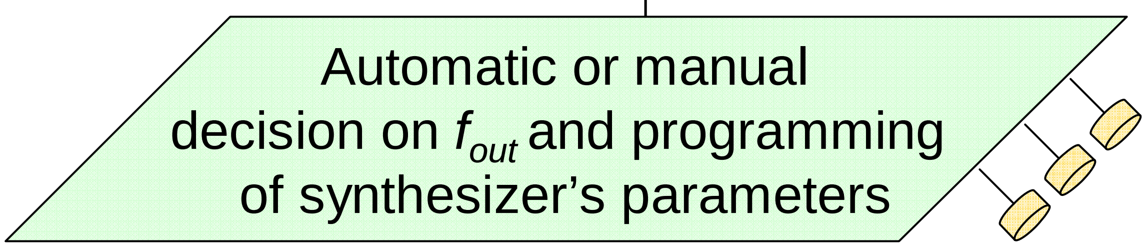
E.g. $f_{osc} = 10 MHz$

It generates another periodic signal of frequency f_{out}

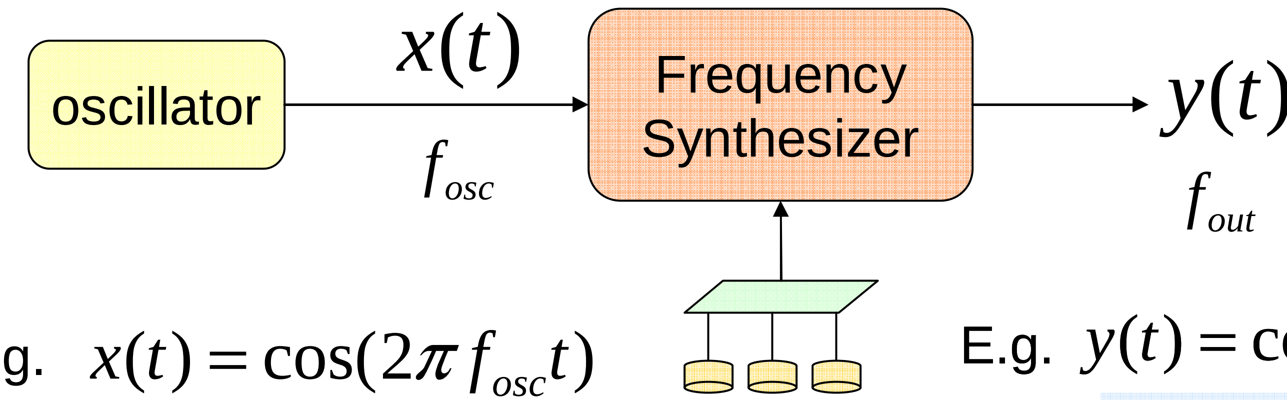


E.g. $y(t) = \cos(2\pi f_{out} t)$

E.g. $f_{out} = 25.4 MHz$



What is **Fine** Frequency Synthesis?



E.g. $x(t) = \cos(2\pi f_{osc} t)$

$f_{osc} = 10 MHz$

E.g. $y(t) = \cos(2\pi f_{out} t)$

$f_{out} = 25.412,487,572 ... MHz$

And, in most cases…

we want f_{out} to be adjustable in Small and Uniform Frequency Steps (Frequency Resolution)

$$\begin{array}{rl} & \vdots \\ & 25.412,487,56 \quad MHz \\ f_{out} = & 25.412,487,57 \quad MHz \\ & 25.412,487,58 \quad MHz \\ & 25.412,487,59 \quad MHz \\ & \vdots \end{array}$$

Fine ≠ good!

<u>**Why** do we use Frequency Synthesis?</u>

- **Good** (stable, low noise, etc.) oscillators provide only **one** frequency*

- Finite (and not large) number of frequencies for which one can find a commercially available good oscillator

- <u>Synthesizers</u>: can generate many frequencies
    - their output signal "inherits" good characteristics from the oscillator's signal

- In many applications we need to select among many possible frequencies

---

***** "inconvenient" exceptions exist

Where do we use Frequency Synthesis?

- Almost all electronic products have at least one
  Frequency Synthesizer
  very basic - very complex

(Wireless, Digital, Audio-Video, Computers,….)

- Your computer has several !
  to generate the many clock signals

Where do we use **Fine** Frequency Synthesis?

- Atomic Clocks & Time Keeping Systems

- Scientific Instruments (frequency, time, distance etc)

- Medical systems (MRI – NMR in general)

…

Diophantine Frequency Synthesis* (DFS)

What is it ? : A number theoretic approach to fine frequency synthesis

potentially resulting to : → superb frequency resolution,
→ very clean output signal
→ fast frequency hoping

using : simple and modular hardware implementations.

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its foundation : Diophantine** Equations

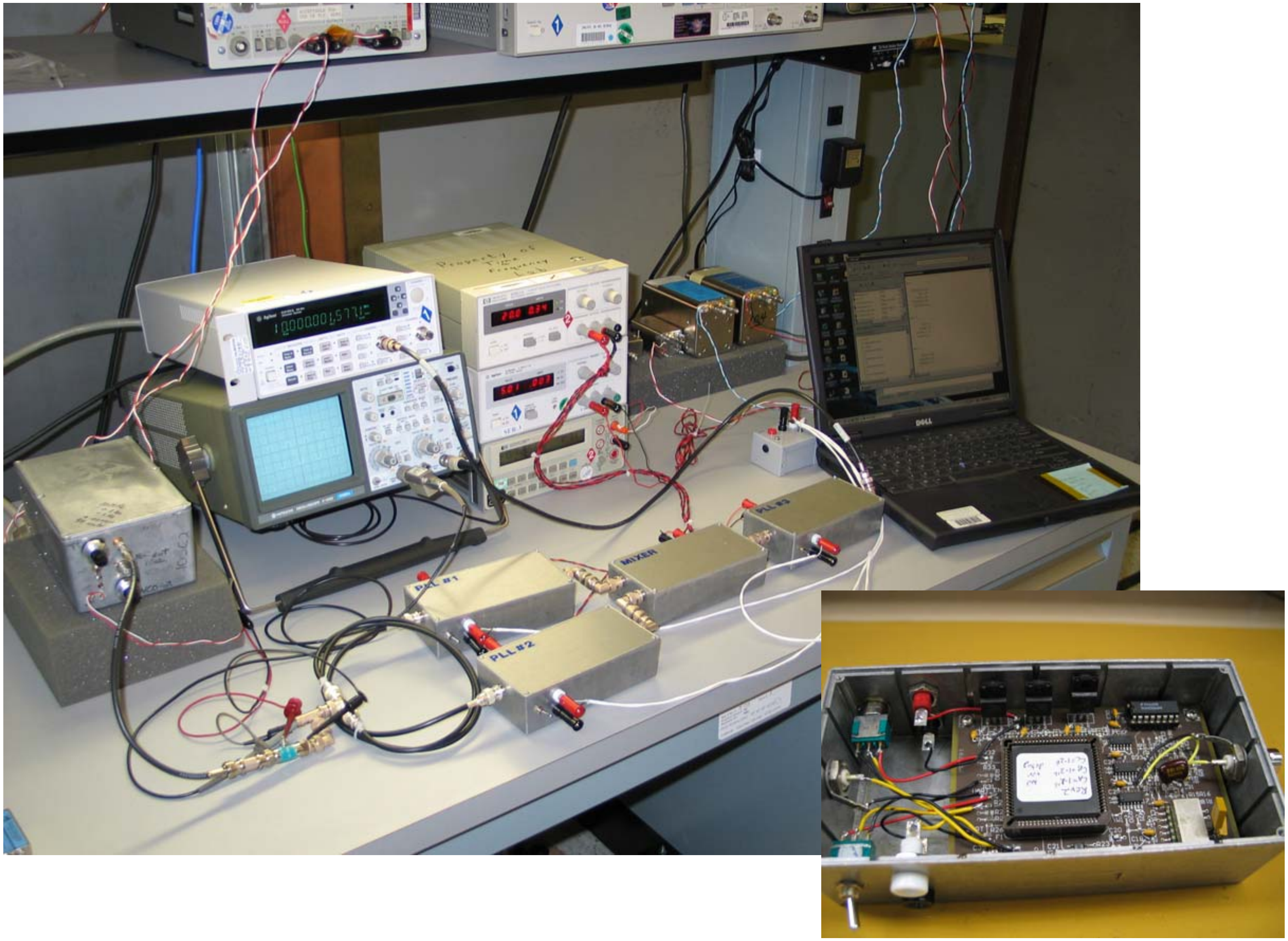
---

working model ? : The APL-JHU team built the first one to demonstrate the mathematical principle.

* *From the great Greek mathematician of antiquity Diophantus, 250 A.D.*

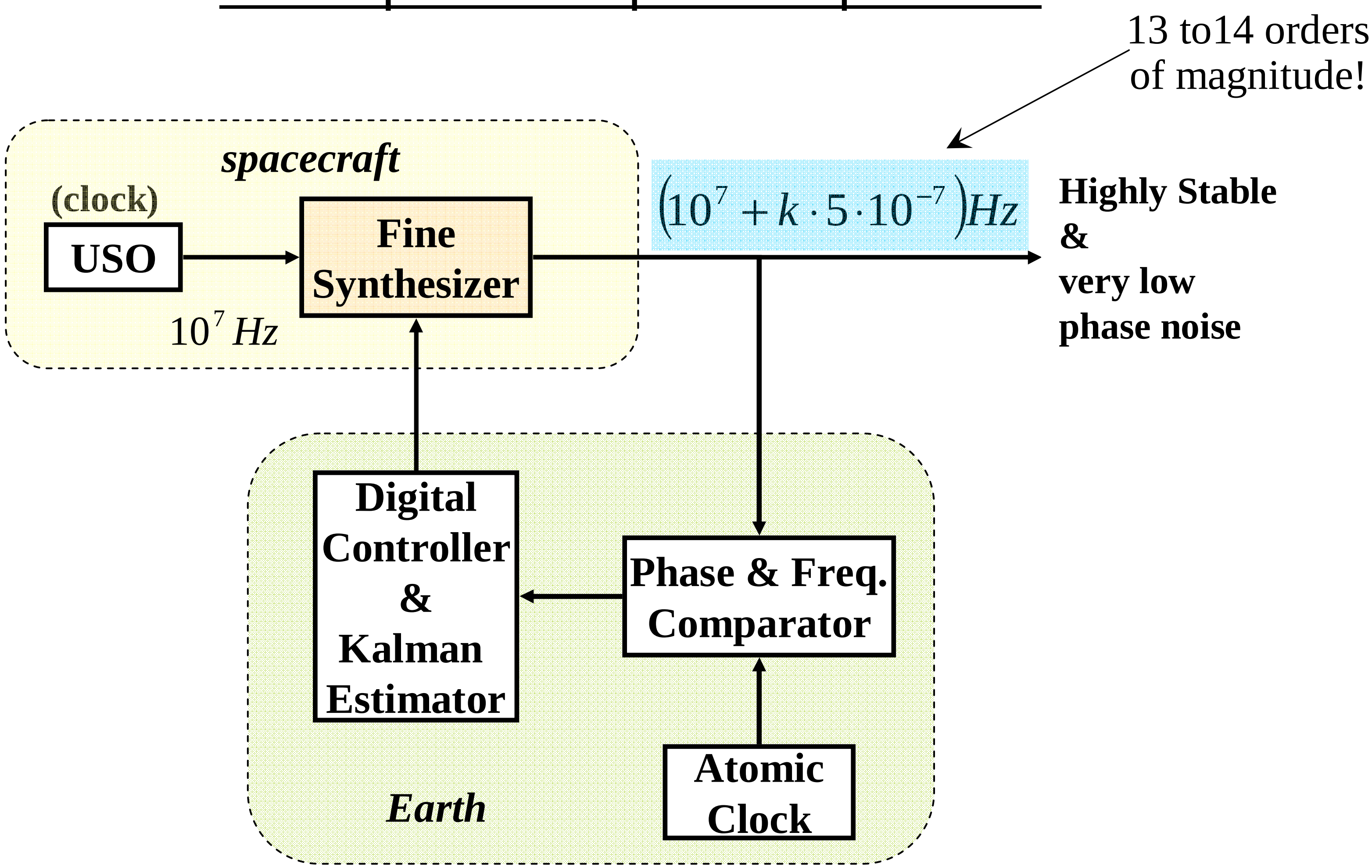
- * *P. Sotiriadis, "Diophantine Frequency Synthesis", IEEE Transactions on UFFC, (To appear).*
- *"Prime-Rational Frequency Synthesis Method and Frequency Synthesizers", P. Sotiriadis, M.L. Edwards, G. Weaver, S. Cheng, D. Loizos, M. Wesley, C. Haskins, patent pending*

The Prototype: Math do work!



Applied Physics Laboratory (APL), J.H.U. Spring 2005.

How Everything Started: Concept of Disciplined Operation



From Gregory Weaver's presentation, APL

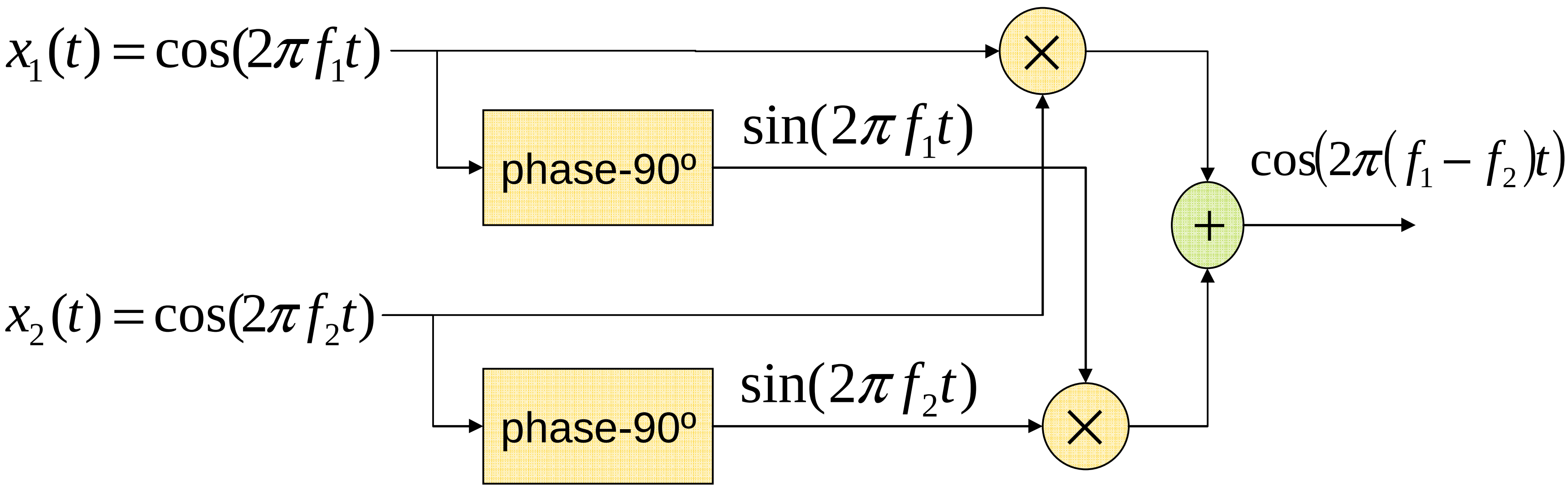
The Basics

of

Frequency Synthesis

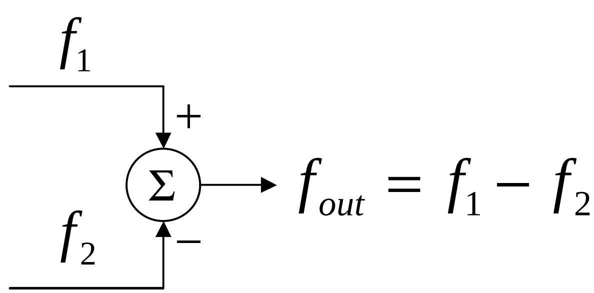
Operations on Periodic Signals

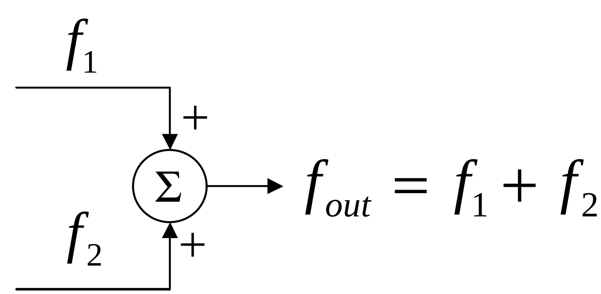
- **Frequency Addition & Subtraction** (one way of doing it…)



$$\cos(2\pi(f_1 - f_2)t) = \cos(2\pi f_1 t)\cos(2\pi f_2 t) + \sin(2\pi f_1 t)\sin(2\pi f_2 t)$$

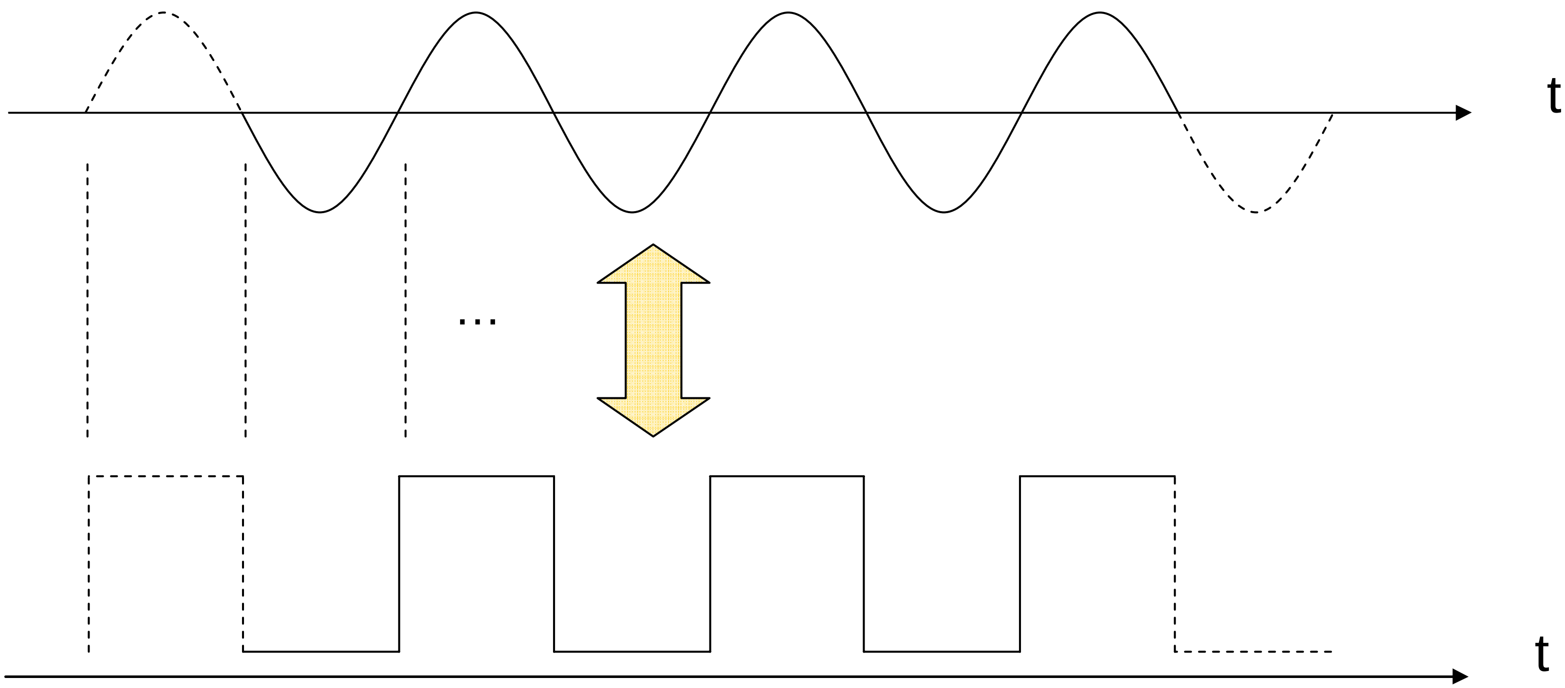
→ Symbol:





Operations on Periodic Signals

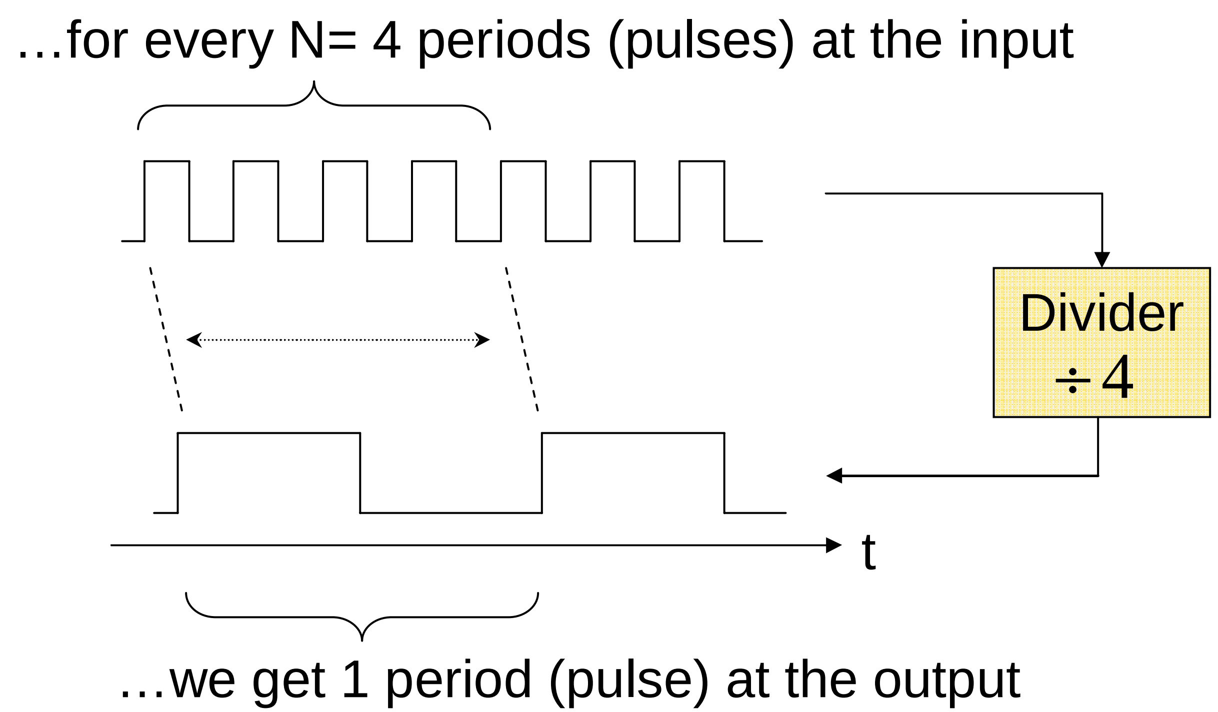
- **Waveform Shaping**



→ Maintain **Frequency** and **Phase** (phase offset possible)

Operations on Periodic Signals

- **Frequency Division** ; done by a **Divider = Counter**

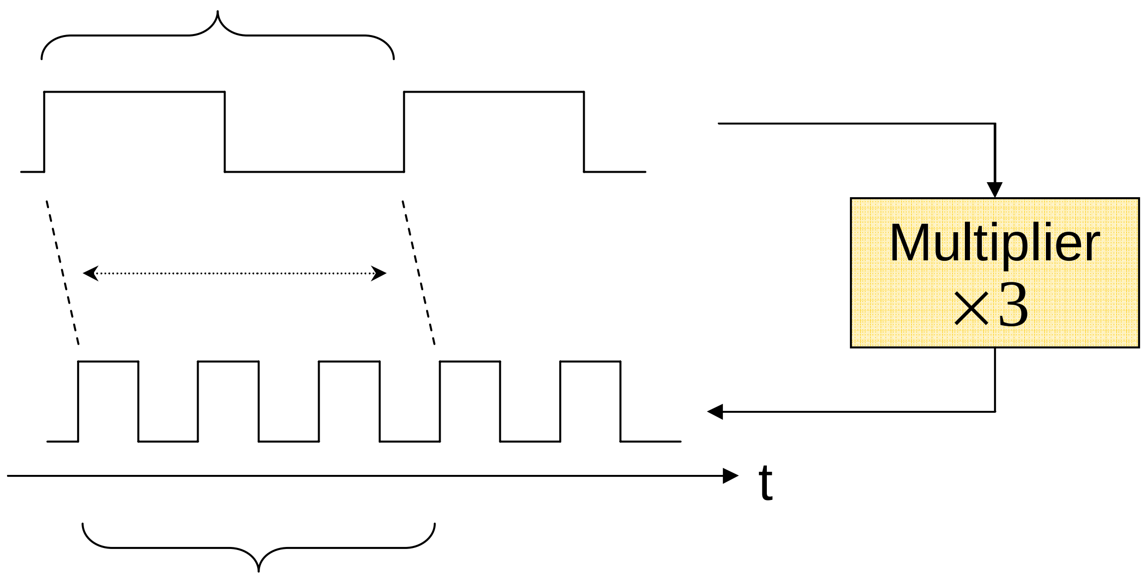


→ Symbol: $f_{in} \longrightarrow \boxed{\div N} \longrightarrow f_{out} = \frac{f_{in}}{N}$ $N \in \mathbb{N}$

Operations on Periodic Signals

- **Frequency Multiplication** ; using Phase-Locked Loop (PLL)

…for every 1 period (pulse) at the input

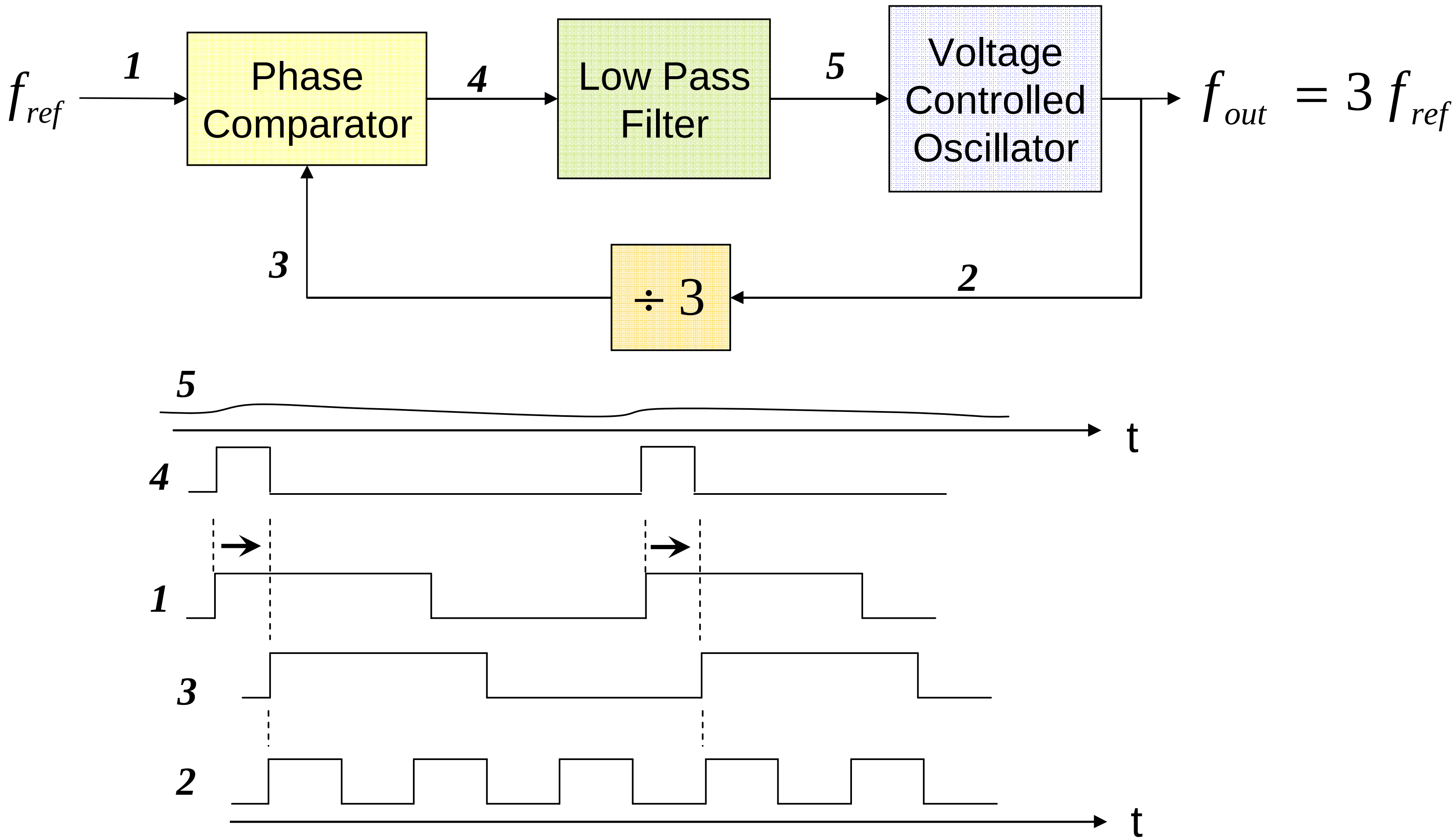


…we get 3 period (pulse) at the output

→ symbol: $f_{in} \longrightarrow \boxed{\times m} \longrightarrow f_{out} = m\ f_{in}$ $m \in \mathrm{N}$

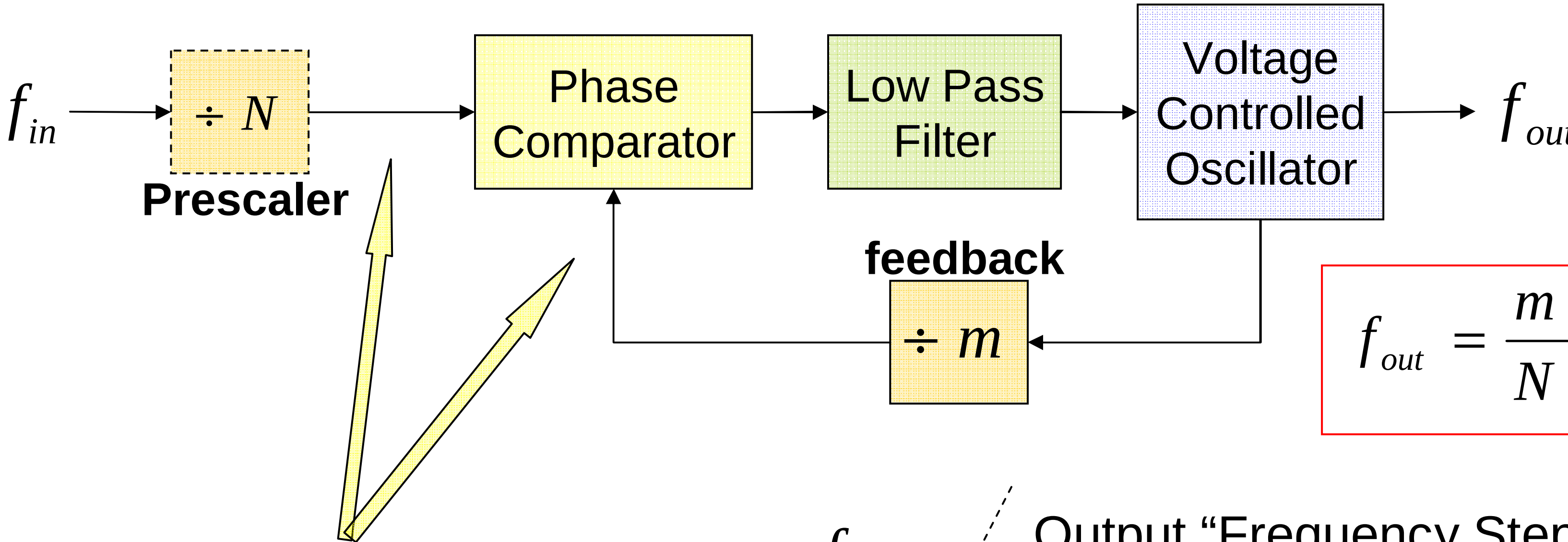
Operations on Periodic Signals

- **The Phase-Locked Loop (PLL)** (Nonlinear Dynamical System)



Operations on Periodic Signals

- **The Phase-Locked Loop (PLL)** - complete -



$$f_{out} = \frac{m}{N} f_{in}$$

"Phase-Comparator Frequency" : $= \dfrac{f_{in}}{N}$

Desirable: $\dfrac{f_{in}}{N}$: **LARGE***

Also Desirable: N : FIXED*
m : Variable

Output "Frequency Step" (Resolution) :

$$m \rightarrow m+1 \Rightarrow \Delta f_{out} = \frac{f_{in}}{N}$$

Desirable: $\dfrac{f_{in}}{N}$: **SMALL**

* For filtering and stability issues

Phase-Locked Loop (PLL) : summary

PLL → frequency multiplication by a RATIONAL number

$$f_{in} \rightarrow \boxed{\times \frac{m}{N}} \rightarrow f_{out}$$

Note: $\frac{n}{N} \neq \frac{k \cdot n}{k \cdot N}$

"Phase-Comparator Frequency" = "Frequency Step" = $\Delta f_{out} = \frac{f_{in}}{N}$

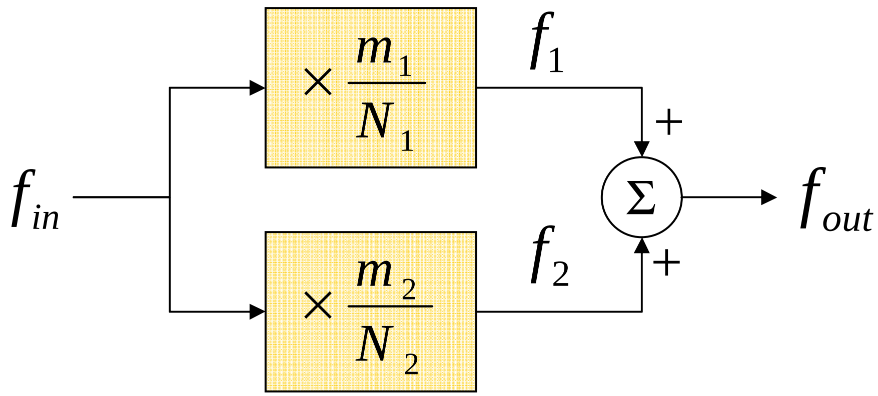
Desirable: $\frac{f_{in}}{N}$: **LARGE**

Desirable: $\frac{f_{in}}{N}$: **SMALL**

} one PLL is NOT enough !

→ Lets try to use 2 PLLs

2 PLLs ????



- Suppose that N_1, N_2 are sufficiently **SMALL** so that the phase-comparator frequencies : $\frac{f_{in}}{N_1}, \frac{f_{in}}{N_2}$ of both PLLs are sufficiently large. ✓
- Suppose that N_1, N_2 are **FIXED (we choose them)** ✓
- What is the Frequency step (Resolution) of f_{out} ?

…if we can make this Small,….. we have (almost) all we want!

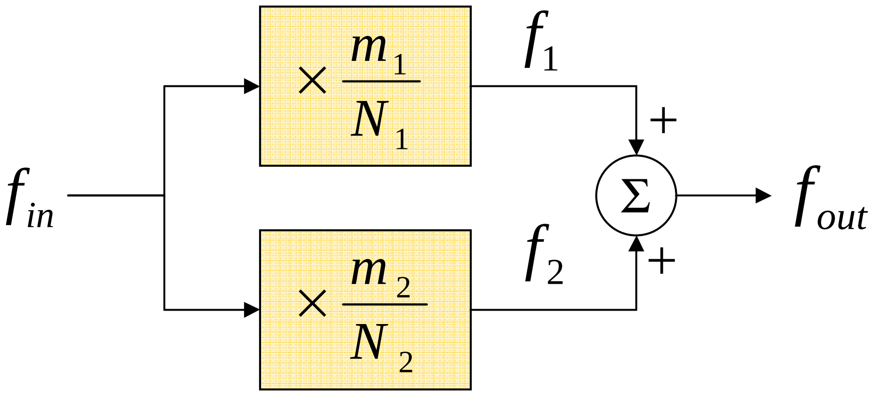
Putting

Number Theory

to

Work

2 PLLs - The New Idea



$$f_{out} = \left(\frac{m_1}{N_1} + \frac{m_2}{N_2} \right) f_{in}$$

$$= \frac{m_1 N_2 + m_2 N_1}{N_1 N_2} f_{in}$$

→ Allow for the moment m_1, m_2 to take non-positive values too.

Theorem*: *Given an integer a, the Diophantine equation*

$$m_1 N_2 + m_2 N_1 = a$$

has a solution (m_1, m_2) *if and only if* $\gcd(N_1, N_2) | a$.

$$a = r \cdot \gcd(N_1, N_2) \Longrightarrow f_{out} = r \cdot \frac{\gcd(N_1, N_2)}{N_1 N_2} f_{in} \quad , \quad r = 0, \pm 1, \pm 2, \ldots$$

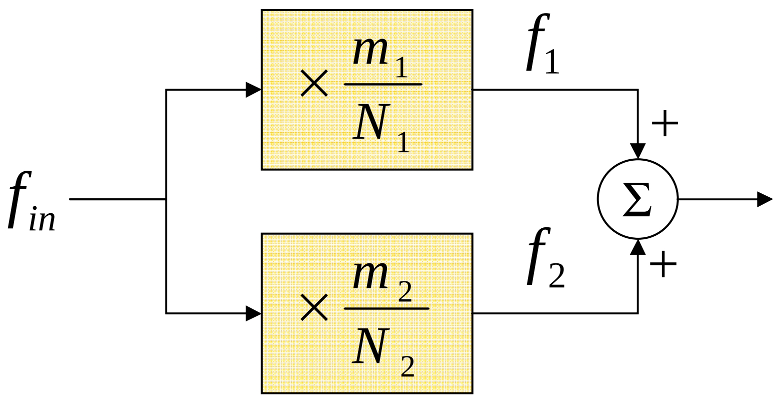
the (output) Frequency Step

* $N_1 \mathrm{Z} + N_2 \mathrm{Z} = \gcd(N_1, N_2) \mathrm{Z}$

2 PLLs - The New Idea

Summarizing:

…if N_1, N_2 : **Pairwise Relatively Prime**, i.e. $\gcd(N_1, N_2) = 1$



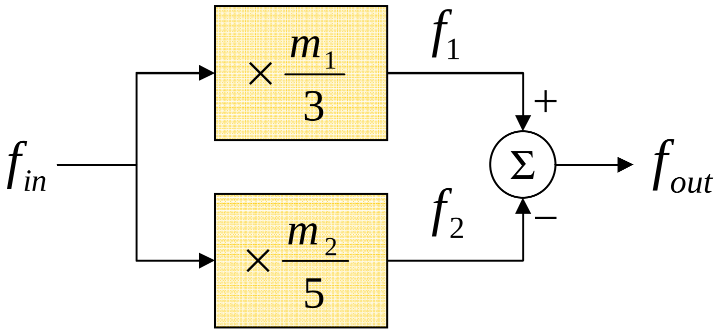
$$f_{out} = r \cdot \frac{\gcd(N_1, N_2)}{N_1 N_2} f_{in}$$

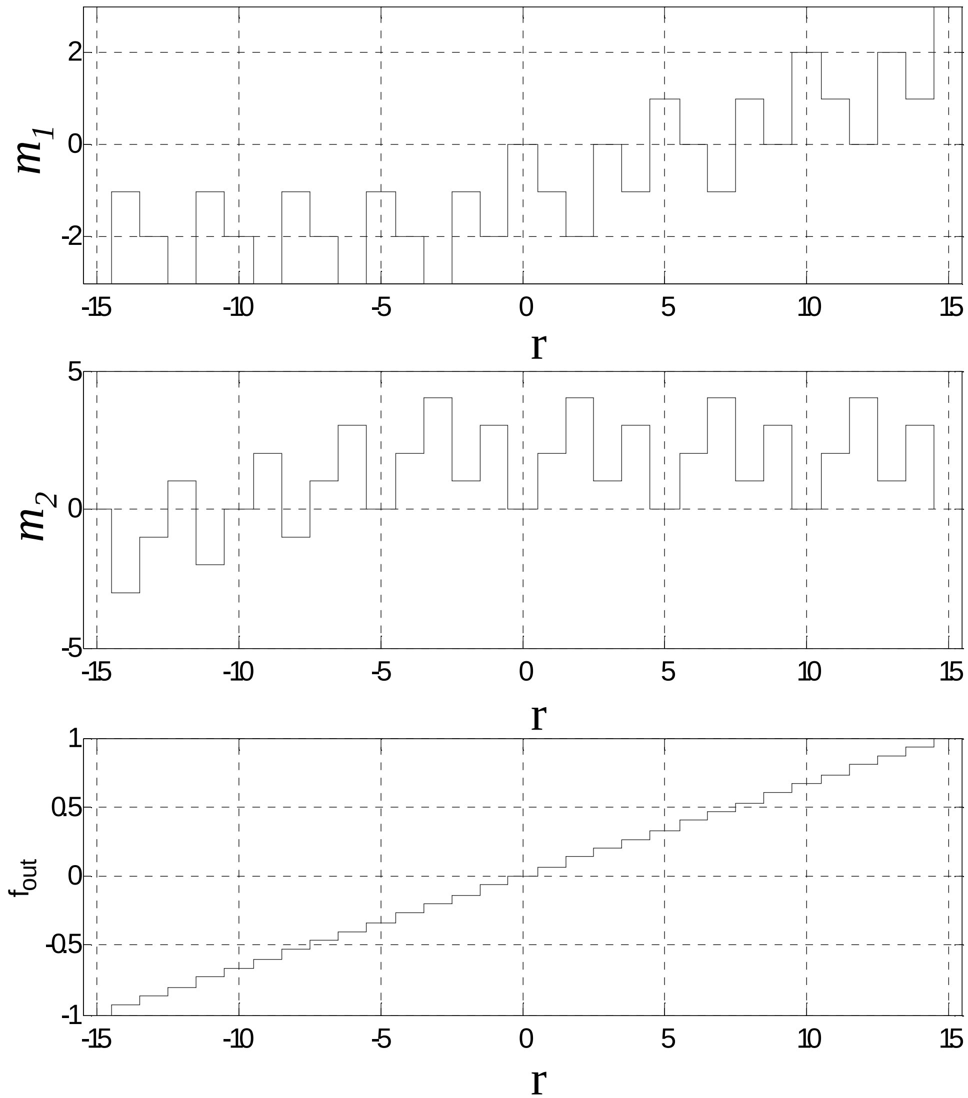
$$= r \cdot \frac{f_{in}}{N_1 N_2}, \quad r = 0, \pm 1, \pm 2, \ldots$$

(output) **Frequency step** << **Phase-comparator frequencies**!

$$\frac{f_{in}}{N_1 N_2} \ll \frac{f_{in}}{N_1}, \frac{f_{in}}{N_2}$$

2 PLLs - Example



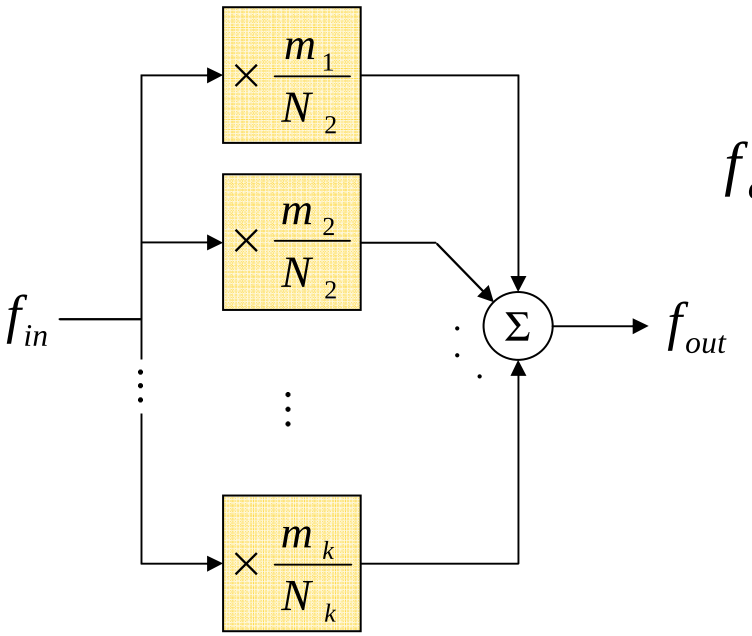


$$f_{out} = r \cdot \frac{\gcd(3,5)}{15} f_{in}$$

$$= r \cdot \frac{f_{in}}{15},$$

$$(f_{in} = 1Hz)$$

Generalization: k - PLLs



$$f_{out} = \left(\frac{m_1}{N_1} + \frac{m_2}{N_2} + \ldots + \frac{m_k}{N_k} \right) f_{in}$$

$$= \frac{m_1 E_1 + m_2 E_2 + \ldots + m_k E_k}{N_1 N_2 \cdots N_k} \cdot f_{in}$$

where: $E_i = \prod_{j \neq i} N_j$

*Theorem**: *Given an integer a, the Diophantine equation*
$m_1E_1 + m_2E_2 + \ldots + m_kE_k = a$
has a solution $(m_1, m_2, \ldots, m_k)$ *if and only if* $\gcd(E_1, E_2, \ldots, E_k) | a$.

$$f_{out} = r \cdot \frac{\gcd(E_1, E_2, \ldots, E_k)}{N_1 N_2 \cdots N_k} f_{in} \quad , \quad r = 0, \pm 1, \pm 2, \ldots$$

The (output) Frequency Step!

Generalization: k - PLLs

Proposition : If $N_1, N_2, \ldots, N_k$ *are* ***pairwise relatively prime***, *i.e.* $\gcd(N_i, N_j) = 1$ *for all* $i \neq j$, *then:*

$$\gcd\Bigg(\underbrace{\prod_{i\neq 1} N_i}_{E_1}, \underbrace{\prod_{i\neq 2} N_i}_{E_2}, \ldots, \underbrace{\prod_{i\neq k} N_i}_{E_k}\Bigg) = 1$$

$\ldots \Rightarrow$ *we can solve* $m_1E_1 + m_2E_2 + \ldots + m_kE_k = a$ *for every* a.

$$f_{out} = \left(\frac{m_1}{N_1} + \frac{m_2}{N_2} + \ldots + \frac{m_k}{N_k}\right) f_{in} = \frac{m_1E_1 + m_2E_2 + \ldots + m_kE_k}{N_1N_2\cdots N_k} \cdot f_{in}$$

$$= r \cdot \frac{f_{in}}{N_1N_2\cdots N_k}, \quad r = 0, \pm 1, \pm 2, \ldots$$

The (output) Frequency Step!

Generalization: k - PLLs

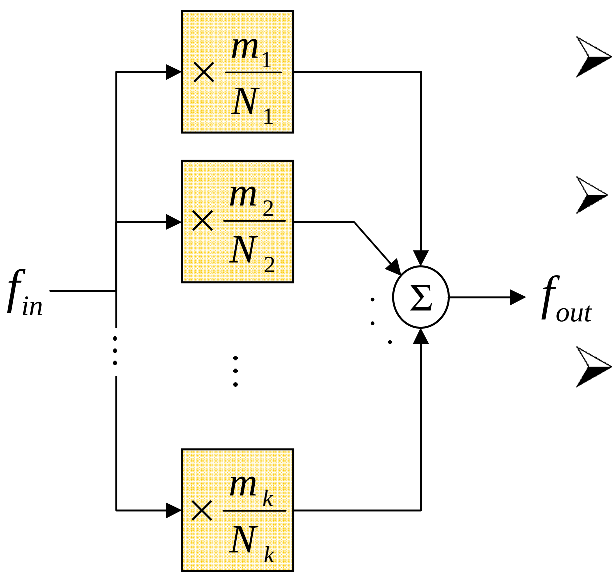
Summarizing:

- Frequency synthesis: ***NEW Idea***

<u>Theorem</u>: *If $N_1, N_2, \ldots, N_k$ are pairwise relatively prime then f_{out} can take all values:*

$$f_{\text{out}} = r \cdot \frac{f_{in}}{N_1 N_2 \cdots N_k} \quad , \qquad r = 0, \pm 1, \pm 2, \ldots$$

i.e. the frequency step is: $f_{in} / (N_1 N_2 \cdots N_k)$

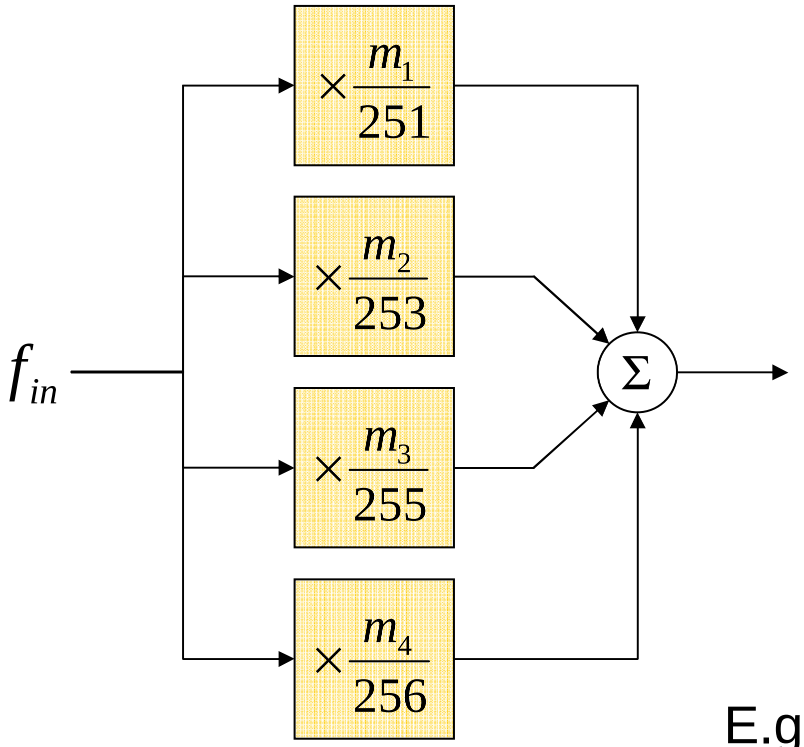


- $N_1, N_2, \ldots, N_k$ *can be* ***Fixed & SMALL*** ✓
- *Phase-Comparator frequencies* $\frac{f_{in}}{N_i}$*:* ***LARGE*** ✓
- The output - Frequency Step $\frac{f_{in}}{N_1 N_2 \cdots N_k}$

  can be ***EXTREMELY SMALL*** ✓

Example: 4 PLLs

251, 253, 255, 256 : Pairwise Relatively Prime



$$N_1 N_2 N_3 N_4 = 4{,}145{,}475{,}840 \cong 4 \cdot 10^9$$

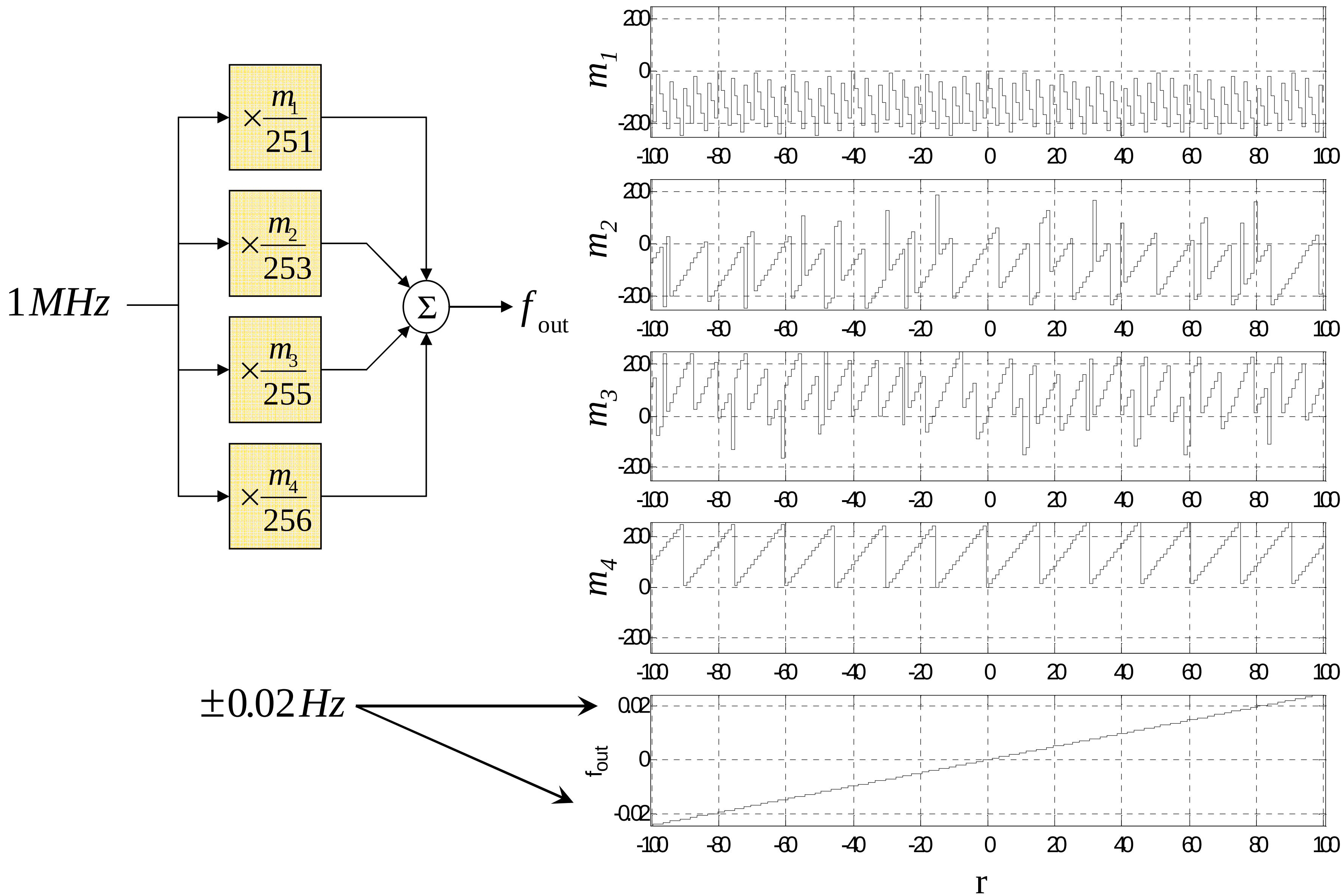
$$f_{out} \cong r \cdot \frac{f_{in}}{4 \cdot 10^9}$$

$$r = -4 \cdot 10^9, \ldots, 4 \cdot 10^9$$

E.g. if $f_{in} = 1MHz$

- Range of f_{out} : $-1MHz, \ldots, +1MHz$
- Frequency Step : $\Delta f_{out} \cong 250 \cdot 10^{-6}\, Hz$

Example: 4 PLLs



Finding the "Right" Solution

Not all solutions of $m_1 E_1 + m_2 E_2 + \ldots + m_k E_k = a \quad (1)$ are "convenient".

→ We want $|m_i|$ Small for all i's.

Note that (1) has many solutions: $\left(E_i = \prod_{j \neq i} N_j \right)$

Proposition: *Let $N_1, N_2, \ldots, N_k$ be pairwise relatively primes, so* $\gcd(E_1, E_2, \ldots, E_k) = 1$. *Then, there exists a (fixed) $k \times k$ integer matrix C, such that, $\det(C) = 1$ and for every a, the complete set of solutions of (1) is:*

$$(m_1, m_2, \ldots, m_k) \in \left\{ C \cdot (a, \rho_1, \rho_2, \ldots, \rho_{k-1})^T : \rho_i \in Z \right\}$$

Finding A "Right" and **Convenient** Solution

Corollary : *If* $N_1, N_2, \ldots, N_k$ *are pairwise relatively prime, then given an integer, a, we can find a solution* $(m_1, m_2, \ldots, m_k)$ of (1) *such that* $-N_i \le m_i \le N_i$ *, for all i's.*

$$m_1 E_1 + m_2 E_2 + \ldots + m_k E_k = a \qquad (1)$$

Moreover, we can do so, in a very computationally efficient way.

Finding A Convenient Solution

$$m_1 E_1 + m_2 E_2 + \ldots + m_k E_k = a \qquad (1)$$

Proof : 1) Solve $x_1 E_1 + x_2 E_2 + \ldots + x_k E_k = 1$

2) ==> $(ax_1, ax_2, \ldots, ax_k)$ is a solution of (1)

3) Note: (1) <=> $\dfrac{m_1}{N_1} + \dfrac{m_2}{N_2} + \ldots + \dfrac{m_k}{N_k} = \dfrac{a}{N_1 N_2 \cdots N_k}$

and set: $y_i = ax_i$ mod N_i, $i=1,2,\ldots,k.$

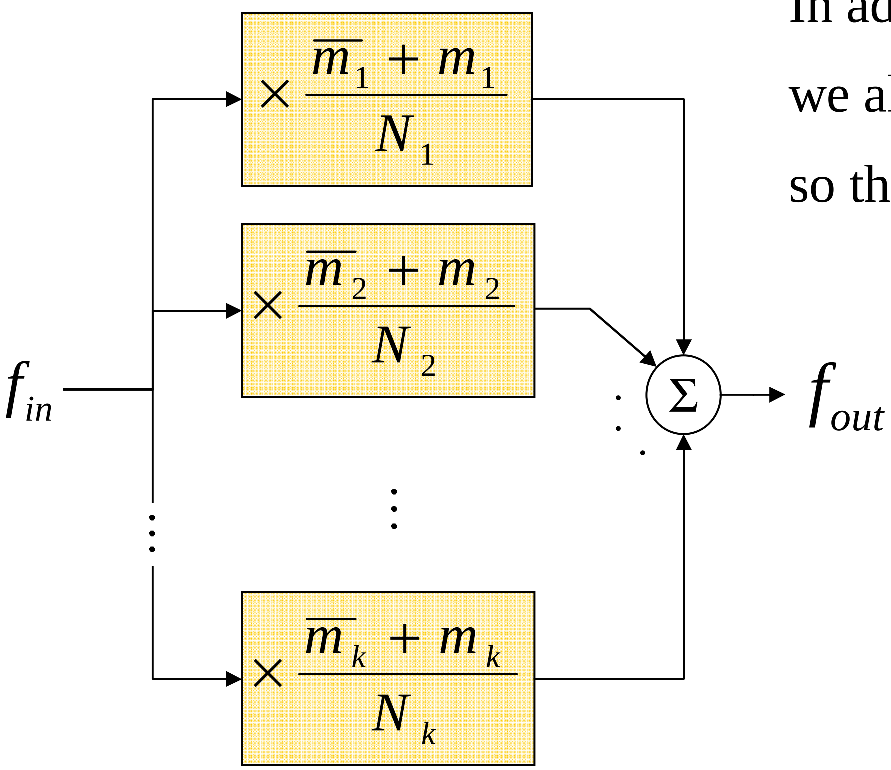
Then: $\dfrac{y_1}{N_1} + \dfrac{y_2}{N_2} + \ldots + \dfrac{y_k}{N_k} = \dfrac{a}{N_1 N_2 \cdots N_k} + q$

with $q \in \{0,1,.., k\}$

4) A desired solution is: $y_1 - N_1, y_2 - N_2, \ldots, y_q - N_q, y_{q+1}, \ldots, y_k.$

Note that $|y_i| \le N_i$ *and* $|y_i - N_i| \le N_i$ *for all i's.*

Fixing the Sign and Relative variation

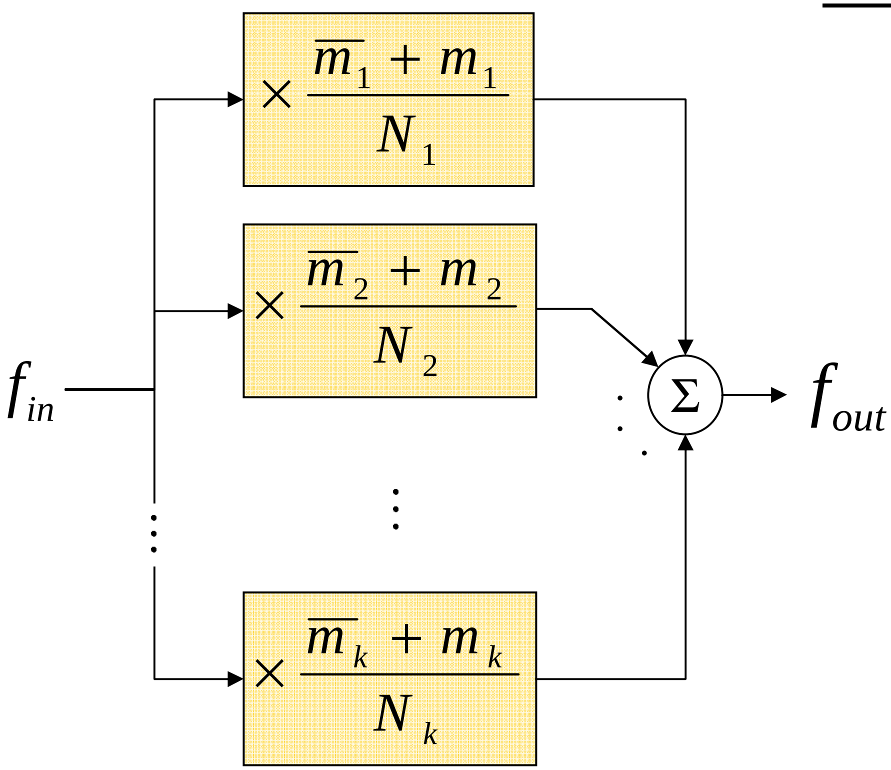


In addition to choosing $N_1, N_2, \ldots, N_k$ we also choose **fixed** $\overline{m}_1, \overline{m}_2, \ldots, \overline{m}_k$ so that:

1) the relative variation of the feedback dividers: $\frac{\overline{m}_i \pm N_i}{\overline{m}_i}$ (pullability of the VCOs) is sufficiently SMALL.

2) The "central" frequency: $\overline{f}_{out} = \left(\frac{\overline{m}_1}{N_1} + \frac{\overline{m}_2}{N_2} + \ldots + \frac{\overline{m}_k}{N_k} \right) f_{in}$ is the appropriate one.

Finally



The phase-comparator frequencies of the PLLs are: $\frac{f_{in}}{N_1}, \frac{f_{in}}{N_2}, \ldots, \frac{f_{in}}{N_k}$

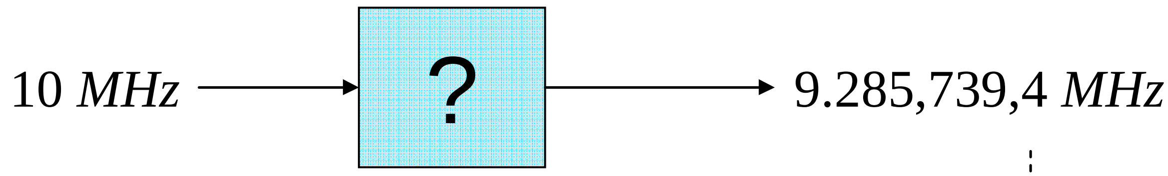
and they can be sufficiently LARGE

while…

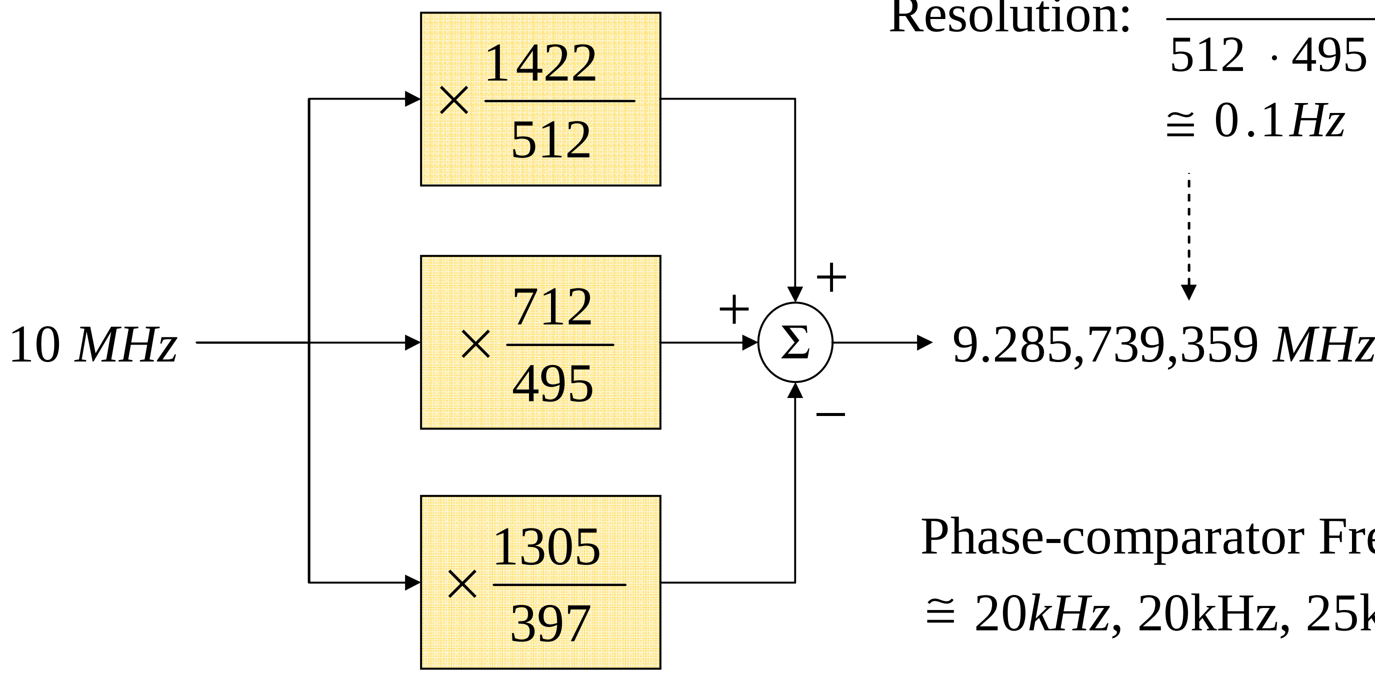
- f_{out} Ranges from: $\overline{f}_{out} - f_{in}$ to $\overline{f}_{out} + f_{in}$
- with Frequency Step (resolution) : $\frac{f_{in}}{N_1 N_2 \cdots N_k}$

Example 1: Fixed Frequency DFS

Problem: **10 *MHz*** signal is **available**, a **9.285,739,4 *MHz*** signal is **needed**.



Resolution: $\dfrac{10\ MHz}{512 \cdot 495 \cdot 397} \cong 0.1Hz$

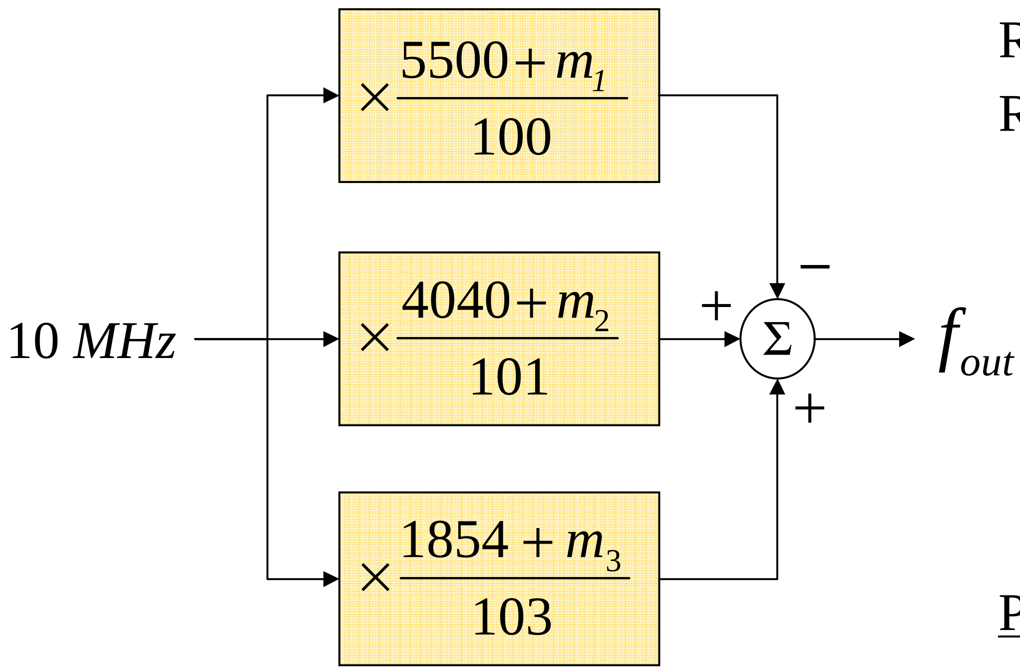


Phase-comparator Frequencies:

$\cong$ 20*kHz*, 20kHz, 25kHz

Example 2: Variable Frequency DFS

Problem: **1 *MHz*** available, **2 *MHz* - 4 *MHz*** with step <1*Hz* is **needed**.



Output Frequency f_{out}

Range: $2MHz$ to $4MHz$

Resolution: $\cong 1Hz$

$$-100 \le m_1 \le 100$$
$$-101 \le m_2 \le 101$$
$$-103 \le m_3 \le 103$$

Phase-comparator

Frequencies: $\cong$ 10 *kHz*

Solving the Diophantine Equations

$$m_1 N_2 + m_2 N_1 = a$$ ⇒ Euclid's algorithm

$$m_1 E_1 + m_2 E_2 + \ldots + m_k E_k = a$$ ⇒ Decompose it into a sequence of k-1 equations on two variables

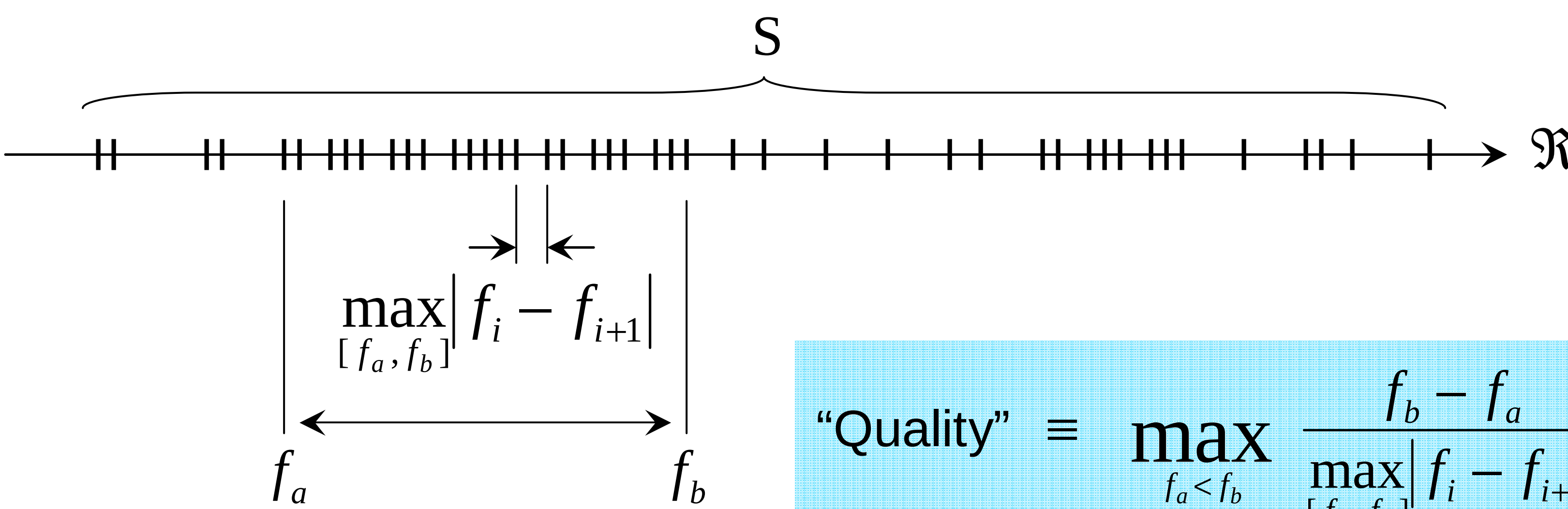
- Using MATLAB : Prefer Variable Precision Arithmetic (VPA)
- Binary Tree decomposition of $m_1 E_1 + m_2 E_2 + \ldots + m_k E_k = a$ allows for minimizing the size of all integers used in the intermediate calculations ✓
- Fast algorithms allow for searching for "best sets" of pairwise relatively prime integers ✓

Diophantine Frequency Synthesis

- The essence of the problem:

$$f_{out} = F\left(p_1, p_2, \ldots, p_k\right) \cdot f_{in}$$

- By varying the parameters , p_1 , p_2,…, p_k , within acceptable intervals, we generate a SET, S, of frequencies f_{out}



"Quality" $\equiv \max_{f_a < f_b} \dfrac{f_b - f_a}{\max_{[f_a, f_b]} |f_i - f_{i+1}|}$

…of F & constraints on p_1 , p_2,…, p_k

Diophantine Frequency Synthesis

- Extensions
  - Problems to be Solved - 1

Quality of $f_{out} = \left(\frac{m_1}{N_1} + \frac{m_2}{N_2} \right) f_{in}$ by varying numerators & denominators ?

$$m_{\min} < m_i \leq m_{Max}$$

$$N_{\min} < N_i \leq N_{Max}$$

Given: x>0 (real) minimize: $\left| \frac{m_1}{N_1} + \frac{m_2}{N_2} - x \right|$

$$m_{\min} < m_i \leq m_{Max}$$

$$N_{\min} < N_i \leq N_{Max}$$

"Extension" of the **continued fraction** approximation???

Diophantine Frequency Synthesis

- Extensions
  - Problems to be Solved - 2

Extend Problem 1 to k- Fractions

Diophantine Frequency Synthesis

- Extensions
  - Problems to be Solved - 3

Quality of $f_{out} = \frac{m_1}{N_1} \cdot \frac{m_2}{N_2} \cdot f_{in}$ by varying numerators & denominators ?

$$m_{\min} < m_i \le m_{Max}$$
$$N_{\min} < N_i \le N_{Max}$$

Given: x>0 (real) minimize: $\left| \frac{m_1}{N_1} \cdot \frac{m_2}{N_2} - x \right|$

$$m_{\min} < m_i \le m_{Max}$$
$$N_{\min} < N_i \le N_{Max}$$

Something like **continued fraction** approximation???

Diophantine Frequency Synthesis

- Extensions
  - Problems to be Solved - 4

Extend Problem 3 to k- Products

Diophantine Frequency Synthesis

- Extensions
  - Problems to be Solved - 5

Quality of $$f_{out} = \left(1 \pm \frac{1}{N_1}\right)\left(1 \pm \frac{1}{N_2}\right)\cdots\left(1 \pm \frac{1}{N_k}\right)\cdot f_{in}$$?

$$N_{\min} < N_i \le N_{Max}$$

choose any combination of signs
(and keep it fixed)

Given: x>0 (real) minimize: $$\left|\left(1 + \frac{1}{N_1}\right)\left(1 - \frac{1}{N_2}\right)\cdots\left(1 - \frac{1}{N_k}\right) - x\right|$$

$$N_{\min} < N_i \le N_{Max}$$

Thank You